In the outstanding Office Action, Claims 1-4, 6-8, 10-13, 15-17 and 19 were rejected under 35 U.S.C. § 102(b) as anticipated by Matsuda; Claims 5, 14 and 19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsuda; and Claims 9 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsuda.

Applicants thank the Examiner for the courtesy of an interview extended to Applicants' representative on March 27, 2003. During the interview, the differences between the present invention and the applied art were discussed. No agreement was reached pending the Examiner's further review when a response is filed. Arguments presented during the interview are reiterated below.

Claims 1-4, 6-8, 10-13, 15-17 and 19 stand rejected under 35 U.S.C. § 102(b) as anticipated by Matsuda. This rejection is respectfully traversed.

Amended Claim 1 is directed to a semiconductor device including at least three power terminals provided one above the other, and at least one semiconductor chip having a first main surface and a second main surface opposite and parallel to the first main surface. Further, the first and second main surfaces are sandwiched between and in parallel with a predetermined two power terminals of the at least three power terminals such that the first and second main surfaces of the at least one semiconductor chip are electrically connected to the predetermined two power terminals without bonding wires. Independent Claim 11 includes similar features.

In a non-limiting example, Figure 1B illustrates at least one semiconductor chip 11 having a first main surface 13 (i.e., an emitter surface) and a second main surface opposite and parallel to the first main surface (i.e., a collector surface of the chip 11). Further, as shown, the first and second main surfaces are sandwiched between and in parallel with a predetermined two power terminals 3, 8 of the at least three power terminals 3, 4 and 8 such

that the first and second main surfaces of the at least one semiconductor chip 11 are electrically connected to the predetermined two power terminals 3, 8 without bonding wires.

As noted in the background of the invention, in a conventional module structure as shown in Figure 9A, the external power terminal 61 is connected with chips 65, 66 through a bonding wire 64. Consequently, wire resistance caused by the bonding wire 64 and self-inductance increase (see page 2, lines 8-13). The present invention solves these problems by providing the claimed semiconductor device not using bonding wires, which considerably reduces to voltage drop due to the internal wiring, because the connection between the semiconductor chips and the power terminals is realized by a short distance through the surface of the chips (see page 3, lines 5-9).

The outstanding Office Action states Matsuda teaches the claimed invention. However, as shown in Figure 2, the first and second main surfaces of the transistor 29 or diode 31 (i.e., the top and bottom surfaces) are not sandwiched between and in parallel with a predetermined two power terminals such that the first and second main surfaces are electrically connected to the predetermined two power terminals without bonding wires. Rather, the top surfaces (i.e., main surfaces of the chips) are connected to the power terminals via Al bonding wires 35. Thus, the problems noted by the present invention occur in Matsuda.

In addition, during the interview, the Examiner explained that the side surfaces of the transistor 29 could be interpreted as top and bottom surfaces. However, it is respectfully submitted that the side surfaces of the transistor 29 are not equivalent to first and second main surfaces as claimed by the present invention. In addition, as shown in Figure 2, the top main surface of the transistor 29 is connected to the power terminal via the bonding wires 35.

Accordingly, it is respectfully submitted independent Claims 1 and 11 and each of the claims depending therefrom are allowable.

Further, regarding the additional rejections noted in the outstanding Office Action, it is respectfully requested these rejections also be withdrawn as the claims rejected therein are dependent claims.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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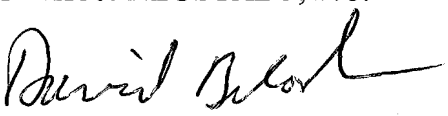

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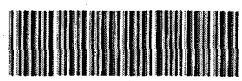

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IN THE CLAIMS

--1. (Four Times Amended) A semiconductor device comprising:

at least three power terminals provided one above the other; and

at least one semiconductor chip having a [top] first main surface and a [bottom] second main surface opposite and parallel to the first main surface, said first and second main surfaces being sandwiched between and in parallel with [and interposed between] a predetermined two power terminals of said at least three power terminals [in a direction intersecting the top surface and the bottom surface, with], such that the [top and bottom] first and second main surfaces of the at least one semiconductor chip are electrically connected to the predetermined two power terminals without bonding wires.

11. (Twice Amended) A semiconductor device comprising:

at least three power terminals provided one above another; and

at least one semiconductor chip having a [top] first main surface and a [bottom] second main surface opposite and parallel to the first main surface, said first and second main surfaces being sandwiched between and in parallel with [and interposed between] a predetermined two power terminals of said at least three power terminals [in a direction intersecting the top surface and the bottom surface, with], such that the [top and bottom] first and second main surfaces of the at least one semiconductor chip are electrically connected to the two power terminals without bonding wires,

wherein [one face] the first main surface of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and [another face] the second main surface is connected to another power terminal of said two power terminals by soldering or pressure welding.--